8-CHARACTER 4-LINE DOT MATRIX LCD CONTROLLER DRIVER WITH EXTENSION FUNCTION

■ GENERAL DESCRIPTION

The NJU6426 is a Dot Matrix LCD controller driver for 8-character or up to 24-character 4-line with icon display in single or combine with some of extension driver.

It contains voltage converter, bleeder resistance, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers and extension driver interface circuits.

The voltage converter and bleeder resistance generates about twofold voltage(10V) and bias voltage for LCD driving waveform internally from single power supply (5V). Consequently, high-contrast display can be performed though the simple power supply circuits.

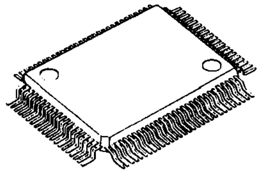
The CR oscillator incorporates C and R, therefore no external components for oscillation are required.

The microprocessor interface circuits which operate by 2MHz, can be connected directly to 4/8bit microprocessor.

The character generator consists of 9,600 bits ROM and 64 bytes RAM.

The 33-common (32 for character, 1 for icon) and 40-segment drivers are operated up to 13.5V, and the icon common driver display up to 40 or 80 icon in single or combine with some of extension driver.

■ PACKAGE OUTLINE



NJU6426F

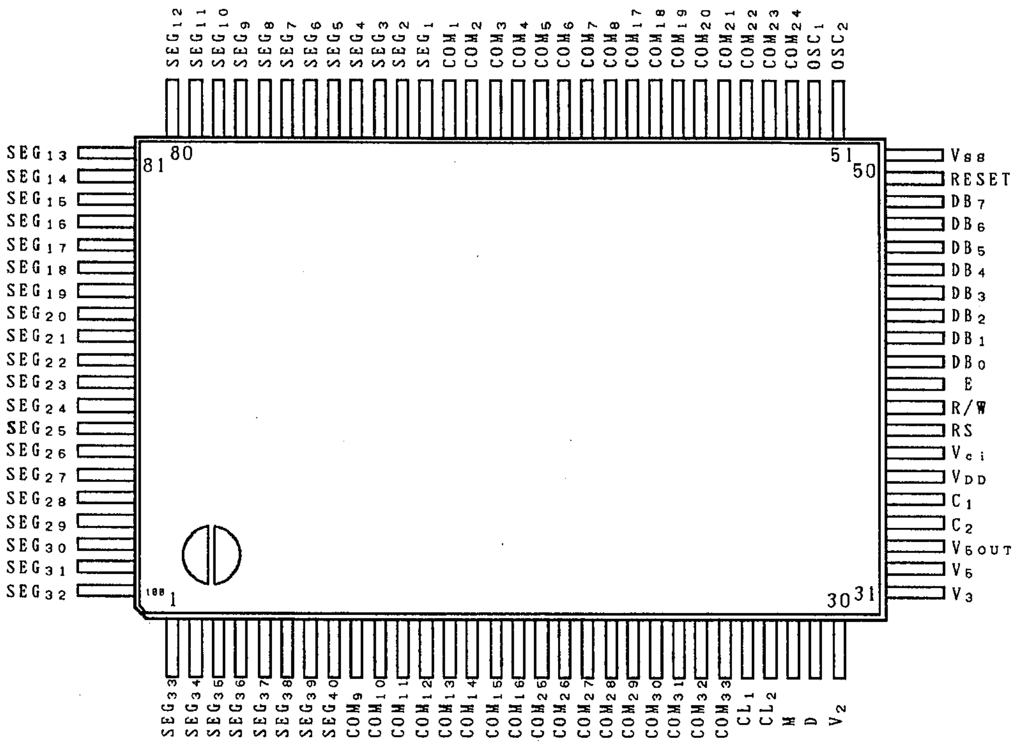
■ FEATURES

- 8-character 4-line Dot Matrix LCD Controller Driver
- Maximum 80 icon Display (Using COM_{33})
- 4/8 Bit Microprocessor Direct Interface
- Display Data RAM - 96 x 8 bits : Maximum 24-character 4-line Display
- Character Generator ROM - 9,600 bits : 240 Characters for 5 x 7 Dots
- Character Generator RAM - 64 x 8 bits : 8 Patterns(5 x 7 Dots)
- High Voltage LCD Driver : 33-common / 40-segment
- Maximum Display Character Number :

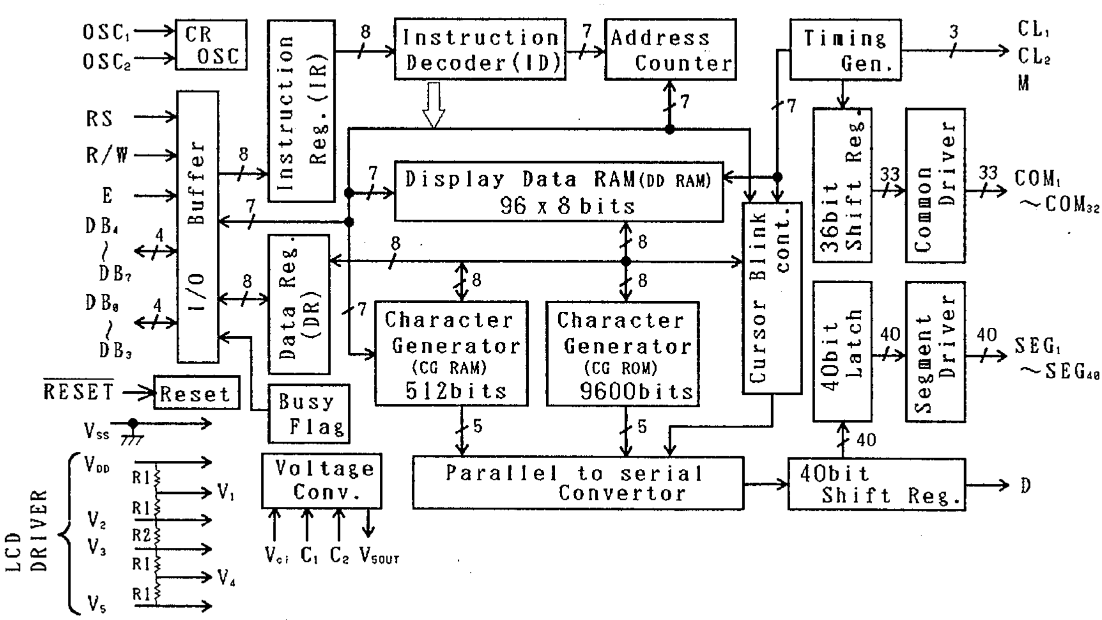
Disp. Line	Ext. Drv	Display Char.	DD RAM	Disp. Line	Ext. Drv	Display Char.	DD RAM
2 Lines	NON	16 Characters	80 x 8 bits	4 Lines	NON	8 Characters	80 x 8 bits
	NJU6407C	24 Characters			NJU6417C	20 Characters	
	NJU6407C	32 Characters			NJU6416 or 6415	24 Characters	96 x 8 bits
	NJU6417C	40 Characters					

- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Extension Function
- Power On Initialize / Hardware Reset Function
- Voltage Converter and Bleeder Resistance On-chip
- Oscillation Circuit On-chip
- Low Power Consumption
- Operating Voltage --- 5 V
- Package Outline --- Chip / QFP 100 / TCP
- C-MOS Technology

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



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■ TERMINAL DESCRIPTION

NO.	SYMBOL	FUNCTION
36	V_{DD}	Power Source (+ 5V)
50	V_{SS}	Power Source (0V)
30,31,32	V_2,V_3,V_5	LCD Driving Voltage Output for Extension Driver and LCD Driving Voltage Adjust Terminals.
52 51	OSC_1 OSC_2	Oscillation Frequency Adjust Terminals. Normally Open. (Oscillation C and R are incorporated, Osc Freq.=330kHz) For external clock operation, the clock should be input on OSC_1.
38	RS	Register selection signal input(Pull-up resistance On-chip) "0" : Instruction Register (Writing) Busy Flag, Address Counter (Reading) "1" : Data Register (Writing/Reading)
39	R/W	Read/Write selection signal input(Pull-up Resistance On-chip) "0" : Write , "1" : Read
40	E	Read/Write activation signal input
45~48	DB_4~DB_7	3-state Data Bus(Upper) to transfer the data between MPU and NJU6426. DB_7 is also used for the Busy Flag reading.
41~44	DB_0~DB_3	3-state Data Bus(Lower) to transfer the data between MPU and NJU6426. These bus are not used in the 4-bit operation.
26	CL_1	Latch Clock Output for Serial Data
27	CL_2	Shift Clock Output for Serial Data
28	M	Alternating signal for LCD Driving Output Terminal
29	D	Serial Data Output Terminal : The serial character pattern data output correspond to the each common signals. "0" - No-active , "1" - Active
68~61 9~16 60~53 17~24	COM_1~COM_8 COM_9~COM_{16} COM_{17}~COM_{24} COM_{25}~COM_{32}	LCD Common Driving Signal If the COM_{17}~COM_{32} are not to be used, please keep it in open
25	COM_{33}	Icon Common Driving Signal
69~100 1 ~ 8	SEG_1~SEG_{32} SEG_{33}~SEG_{40}	LCD Segment Driving Signal
35 34	C_1 C_2	Capacitor for Voltage Doubler Connecting Terminal (+) Capacitor for Voltage Doubler Connecting Terminal (-)
37	V_{ci}	Input Terminal for Voltage Doubler (Normally V_{ci} = V_{DD})
33	V_{5OUT}	Voltage Doubler Output Terminal
49	$\overline{RESET}$	Reset Terminal. When the "L" level input over 1.2ms to this terminal, the system will be reset(f_{OSC}=330kHz)

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Register

The NJU6426 incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Return Home", and address data for Display Data RAM(DD RAM) and Character Generator RAM(CG RAM).
The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).
The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.
The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.
When the address data for the DD RAM or CG RAM is written into the Register(IR), the addressed data in the DD RAM or CG RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.
After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.
These two registers are selected by the selection signal RS as shown below.
Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter(DB_0~DB_6)
1	0	DR	Write (Register(DR) to DD RAM or CG RAM)
1	1		Read (DD RAM or CG RAM to Register(DR))

(1-2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag (BF) is "1", and any instruction reading is inhibited.
The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in Table 1.
The next instruction should be written after the busy flag(BF) goes to "0".

(1-3) Address Counter (AC)

The address counter(AC) addressing the DD RAM and CG RAM.
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.
The address data in the Counter(AC) is output from DB_6~DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1−4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 96 x 8 bits stores up to 96-character display data represented in 8-bit code. Normally, only 80 X 8 bits of the display data RAM (DD RAM) are using and specially 96 X 8 bits are using in 24-character 4-line display.
The unused display data memory area in the DD RAM can be used as a general data memory area. The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.

←Higher order bit　　Lower order bit→

AC	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
	← Hexadecimal →			← Hexadecimal →			

(Example) DD RAM address " 4E "

1	0	0	1	1	1	0
← 4 →			← E →			

(1−4−1) 16-character 2-line Display (N=0, E1=0, E0=0)

The relation between DD RAM address and display position on the LCD is shown below.

NJU6426(COM_1~COM_8)　NJU6426(COM_9~COM_{16})

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd Line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

← DD RAM Address (Hexadecimal)

NJU6426(COM_{17}~COM_{24})　NJU6426(COM_{25}~COM_{32})

Note : In the 2 lines display mode, the 1st and 2nd line address are defined as $(00)_H$ to $(27)_H$ and $(40)_H$ to $(67)_H$. Please note that the end of 1st line address and the beginning of 2nd line address are not consecutive.

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(40)←	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→(0F)
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	→(4F)

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(1－4－2) 24-character 2-line Display (N=0,E1=0,E0=1)...(Extension Driver = NJU6407C)

The relation between DD RAM address and display position on the LCD is shown below:

Upper drivers: NJU6426(COM_1~COM_8) (positions 1–8), NJU6407C (9–12), NJU6426(COM_9~COM_{16}) (13–20), NJU6407C (21–24)

	1	2	3	······	8	9	10	11	12	13	14	15	······	20	21	22	23	24	← Display Position
1st Line	00	01	02	······	07	08	09	0A	0B	0C	0D	0E	······	13	14	15	16	17	← DD RAM Address (Hexadecimal)
2nd Line	40	41	42	······	47	48	49	4A	4B	4C	4D	4E	······	53	54	55	56	57	

Lower drivers: NJU6426(COM_{17}~COM_{24}), NJU6407C, NJU6426(COM_{25}~COM_{32}), NJU6407C

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	······	08	09	0A	0B	0C	0D	0E	0F	······	14	15	16	17	18
(40)←—	41	42	43	······	48	49	4A	4B	4C	4D	4E	4F	······	54	55	56	57	58

(Right Shift Display)

27	00	01	······	06	07	08	09	0A	0B	0C	0D	······	12	13	14	15	16	—→(17)
67	40	41	······	46	47	48	49	4A	4B	4C	4D	······	52	53	54	55	56	—→(57)

(1－4－3) 32-character 2-line Display (N=0,E1=1,E0=0)...(Extension Driver = NJU6407C)

The relation between DD RAM address and display position on the LCD is shown below:

Upper drivers: NJU6426(COM_1~COM_8) (positions 1–8), NJU6407C (9–16), NJU6426(COM_9~COM_{16}) (17–24), NJU6407C (25–32)

	1	2	3	······	8	9	······	16	17	18	19	······	24	25	······	32	← Display Position
1st Line	00	01	02	······	07	08	······	0F	10	11	12	······	17	18	······	1F	← DD RAM Address (Hexadecimal)
2nd Line	40	41	42	······	47	48	······	4F	50	51	52	······	57	58	······	5F	

Lower drivers: NJU6426(COM_{17}~COM_{24}), NJU6407C, NJU6426(COM_{25}~COM_{32}), NJU6407C

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	······	08	09	······	10	11	12	13	······	18	19	······	20
(40)←—	41	42	43	······	48	49	······	50	51	52	53	······	58	59	······	60

(Right Shift Display)

27	00	01	······	06	07	······	0E	0F	10	11	······	16	17	······	1E	—→(1F)
67	40	41	······	46	47	······	4E	4F	50	51	······	56	57	······	5E	—→(5F)

(1－4－4) 40-character 2-line Display (N=0,E1=1,E0=1)...(Extension Driver = NJU6417)

The relation between DD RAM address and display position on the LCD is shown below:

NJU6426(COM_1～COM_8) | NJU6407C | NJU6426(COM_9～COM_{16}) | NJU6407C

	1	2	3	......	8	9	......	20	21	22	23	......	28	29	......	40	← Display Position
1st Line	00	01	02	......	07	08	......	13	14	15	16	......	1B	1C	......	27	← DD RAM Address (Hexadecimal)
2nd Line	40	41	42	......	47	48	......	53	54	55	56	......	5B	5C	......	67	

NJU6426(COM_{17}～COM_{24}) | NJU6407C | NJU6426(COM_{25}～COM_{32}) | NJU6407C

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	......	08	09	......	14	15	16	17	......	1C	1D	......	00	
(40)←—	41	42	43	......	48	49	......	54	55	56	57	......	5C	5D	......	40	

(Right Shift Display)

	27	00	01	......	06	07	......	12	13	14	15	......	1A	1B	......	26	—→(27)
	67	40	41	......	46	47	......	52	53	54	55	......	5A	5B	......	66	—→(67)

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(1－4－5) 8-character 4-line Display (N=1,E0=0)

The relation between DD RAM address and display position on the LCD is shown below:

		1	2	3	4	5	6	7	8	← Display Position
COM_1 ～COM_8	1st Line	00	01	02	03	04	05	06	07	DD RAM Address
COM_9 ～COM_{16}	2nd Line	20	21	22	23	24	25	26	27	← (Hexadecimal)
COM_{17}～COM_{24}	3rd Line	40	41	42	43	44	45	46	47	
COM_{25}～COM_{32}	4th Line	60	61	62	63	64	65	66	67	

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	04	05	06	07	08
(20)←—	21	22	23	24	25	26	27	28
(40)←—	41	42	43	44	45	46	47	48
(60)←—	61	62	63	64	65	66	67	68

(Right Shift Display)

13	00	01	02	03	04	05	06	—→(07)
33	20	21	22	23	24	25	26	—→(27)
53	40	41	42	43	44	45	46	—→(47)
73	60	61	62	63	64	65	66	—→(67)

(1-4-6) 16-character 4-line Display (N=1,EO=0)...(Extension Driver = NJU6407C)

The relation between DD RAM address and display position on the LCD is shown below:

		NJU6426								NJU6407C							
	Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
COM₁ ~COM₈	1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
COM₉ ~COM₁₆	2nd Line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
COM₁₇~COM₂₄	3rd Line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
COM₂₅~COM₃₂	4th Line	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F

← Display Position

← DD RAM Address (Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(20)←—	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
(40)←—	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
(60)←—	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70

(Right Shift Display)

13	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	—→(0F)
33	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	—→(2F)
53	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	—→(4F)
73	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	—→(6F)

(1-4-7) 20-character 4-line Display (N=1,EO=0)...(Extension Driver = NJU6417C)

The relation between DD RAM address and display position on the LCD is shown below:

		NJU6426								NJU6407C				
	Display Position	1	2	3	4	5	6	7	8	9	10	·············	19	20
COM₁ ~COM₈	1st Line	00	01	02	03	04	05	06	07	08	09	·············	12	13
COM₉ ~COM₁₆	2nd Line	20	21	22	23	24	25	26	27	28	29	·············	32	33
COM₁₇~COM₂₄	3rd Line	40	41	42	43	44	45	46	47	48	49	·············	52	53
COM₂₅~COM₃₂	4th Line	60	61	62	63	64	65	66	67	68	69	·············	72	73

← Display Position

← DD RAM Address (Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	04	05	06	07	08	09	0A	··············	13	00
(20)←—	21	22	23	24	25	26	27	28	29	2A	··············	33	20
(40)←—	41	42	43	44	45	46	47	48	49	4A	··············	53	40
(60)←—	61	62	63	64	65	66	67	68	69	6A	··············	73	60

(Right Shift Display)

13	00	01	02	03	04	05	06	07	08	··············	11	12	—→(13)
33	20	21	22	23	24	25	26	27	28	··············	31	32	—→(33)
53	40	41	42	43	44	45	46	47	48	··············	51	52	—→(53)
73	60	61	62	63	64	65	66	67	68	··············	71	72	—→(73)

(1−4−8) 24-character 4-line Display (N=1,E0=1)...(Extension Driver = NJU6416)

The relation between DD RAM address and display position on the LCD is shown below:

		NJU6426							NJU6416						
		1	2	3	4	5	6	7	8	9	········	16	17	········	24 ← Display Position
COM_1 ~COM_8	1st Line	00	01	02	03	04	05	06	07	08	········	0F	10	········	17
COM_9 ~COM_{16}	2nd Line	20	21	22	23	24	25	26	27	28	········	2F	30	········	37 ← DD RAM Address (Hexadecimal)
COM_{17}~COM_{24}	3rd Line	40	41	42	43	44	45	46	47	48	········	4F	50	········	57
COM_{25}~COM_{32}	4th Line	60	61	62	63	64	65	66	67	68	········	6F	70	········	77

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←—	01	02	03	04	05	06	07	08	09	0A	················	17	00
(20)←—	21	22	23	24	25	26	27	28	29	2A	················	37	20
(40)←—	41	42	43	44	45	46	47	48	49	4A	················	57	40
(60)←—	61	62	63	64	65	66	67	68	69	6A	················	77	60

(Right Shift Display)

17	00	01	02	03	04	05	06	07	08	················	15	16	—→(17)
37	20	21	22	23	24	25	26	27	28	················	35	36	—→(37)
57	40	41	42	43	44	45	46	47	48	················	55	56	—→(57)
77	60	61	62	63	64	65	66	67	68	················	75	76	—→(77)

(1－5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character codes.
The storage capacity is up to 240 kinds of 5 x 7 dots character pattern.
The correspondence between character code and standard character pattern of NJU6426 is shown in Table 2-1 and 2-2.
User-defined character patterns (Custom Font) are also available by mask option.

Table 2-1. CG ROM Character Pattern (ROM version -02)

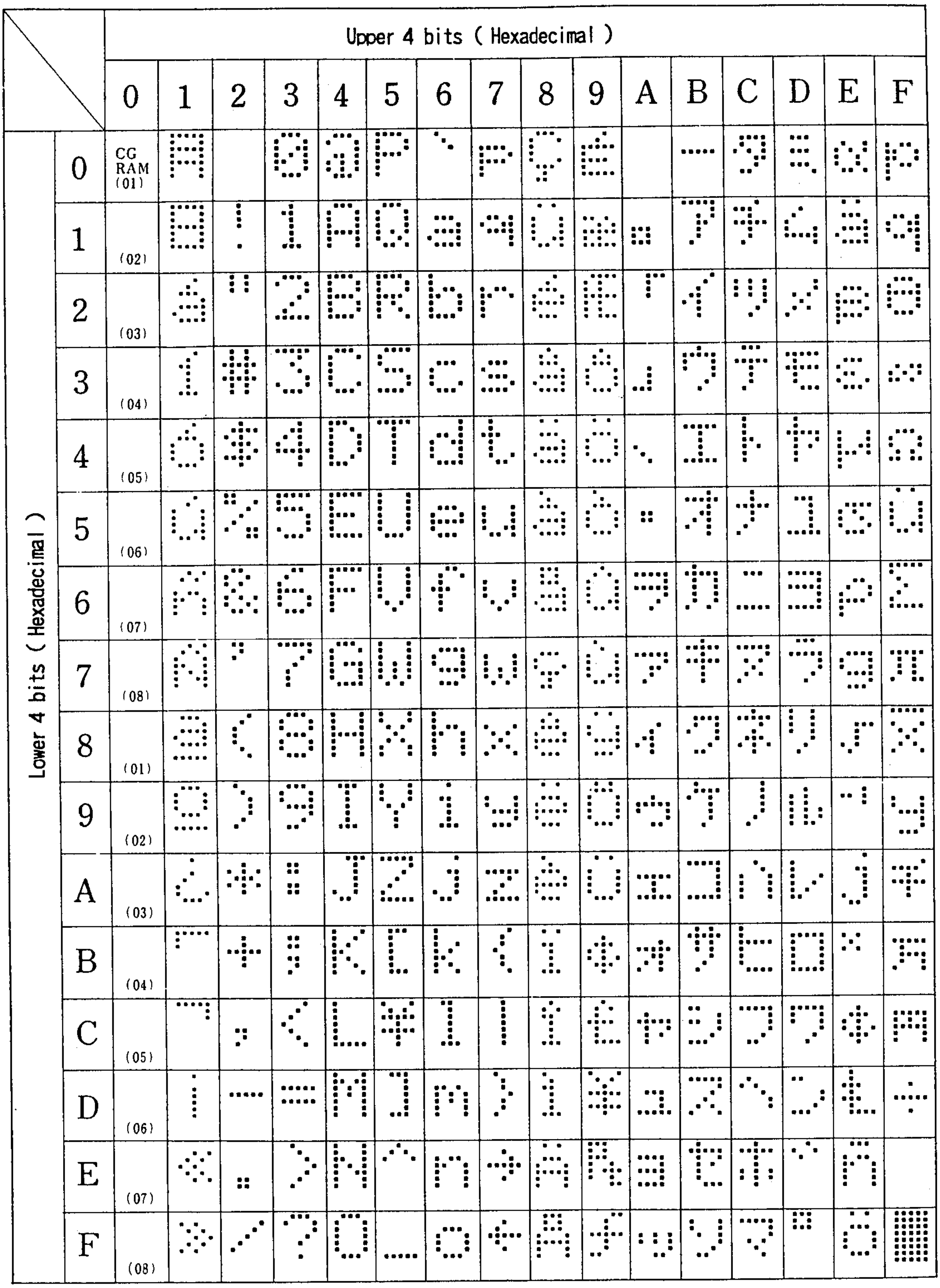

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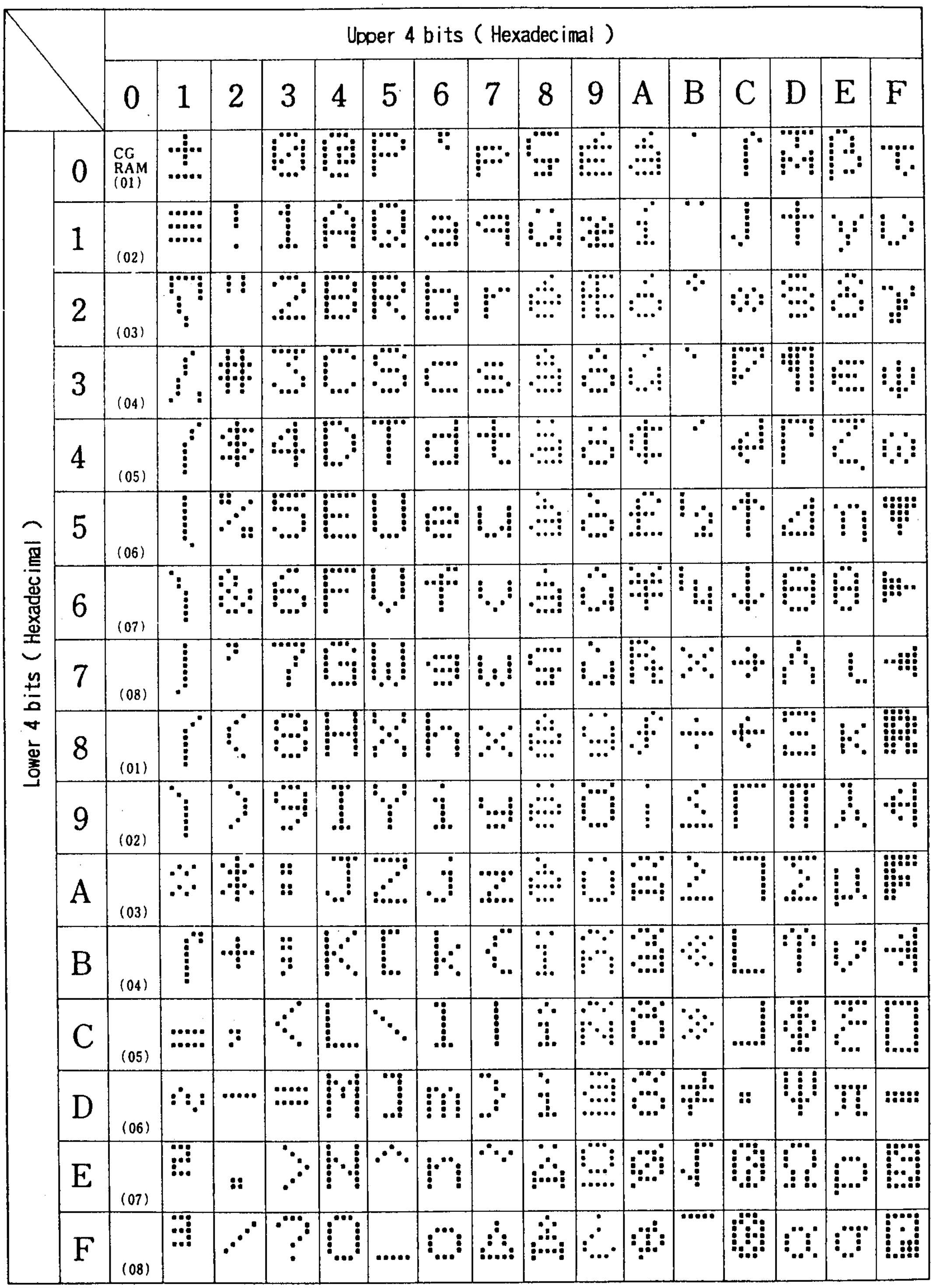
Table 2-2. CG ROM Character Pattern (ROM version -03)



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(1 – 6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern and icon data. The CG RAM can store 8 kind of character in 5 x 7 dots mode or 6 kind of character in 5 x 7 dots mode and icon data.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(07)_H$ or $(08)_H$ - $(0F)_H$ should be written to the DD RAM as shown in Table 2-1 and 2-2.

Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Unused memory area of the CG RAM can also be used as the general data memory area.

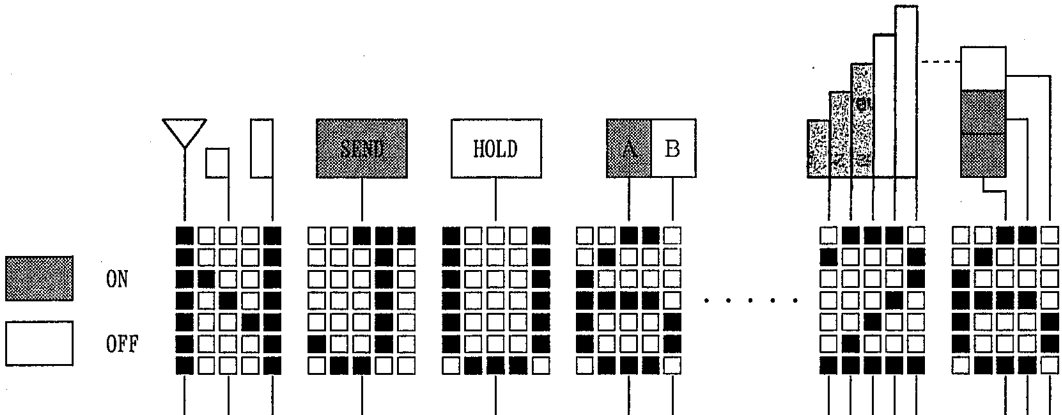
Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots).

Character Code (DD RAM Data)	CG RAM Address		Character Pattern (CG RAM Data)		
7 6 5 4 3 2 1 0 ←Upper bit Lower bit→	5 4 3 ←Upper bit	2 1 0 Lower bit→	7 6 5 ←Upper bit	4 3 2 1 0 Lower bit→	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	
		0 0 1	↑	1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	Character Pattern Example(1)
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0	↓	1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	←Cursor Position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	
		0 0 1	↑	0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	Character Pattern Example(2)
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0	↓	0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	←Cursor Position
		0 0 0	* * *		
		0 0 1	↑		
⋮	⋮	⋮	⋮		
0 0 0 0 * 1 1 1	1 1 1				
		1 0 0			* : Don't Care
		1 0 1	↓		
		1 1 0			
		1 1 1	* * *		

Notes :
1. Character code bit 0 to 2 correspond to the CG RAM add. 3 to 5(3bits:8 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above. The bits 5 to 7 of the CG RAM are not appear on the display (no meaning for the display), but memory elements are existing, therefore it can be used as the general purpose RAM.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 to 2. Therefore, the address $(00)_H$ and $(08)_H$, $(01)_H$ and $(09)_H$, -------, $(07)_H$ and $(0F)_H$ select the same character pattern as shown in Table 2-1 and 2-2.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.
6. CG RAM address $(30)_H$ to $(3F)_H$ are using for both of character pattern memory and icon data memory.

(1－7) Icon Display Function

The NJU6426 can display not only 5 x 7 bits character pattern but also maximum 80 icons.
The icon can display by writing bit "1" to each data bit 0 to 4 in the address $(30)_H$ ～ $(3F)_H$ of CG RAM.
The icon display data is not affected except CG RAM writing and display ON/OFF instruction.
The relation between CG RAM address and icon display position on the LCD is fixed even if the display shift is executed. The relation is shown below:



SEG/display	1 2 3 4 5	6 7 8 9 10	11 12 13 14 15	16 17 18 19 20	・・・・	71 72 73 74 75	76 77 78 79 80
COMMK	$3F_4$～$3F_0$	$3E_4$～$3E_0$	$3D_4$～$3D_0$	$3C_4$～$3C_0$	・・・・	31_4～31_0	30_4～30_0

Note1) The $3F_4$ corresponds bit 4 of $(3F)_H$ in CG RAM.

< CG RAM vs. SEG terminal for icon display >

CG RAM address	data 76543210	SEG terminal
30	***00110	76～80
31	***11100	71～75
32	***00000	66～70
33	***00000	61～65
34	***00000	56～60
35	***00000	51～55
36	***00000	46～50
37	***00000	41～45
38	***00000	36～40
39	***00000	31～35
3A	***00000	26～30
3B	***00000	21～25
3C	***00100	16～20
3D	***00000	11～15
3E	***00100	6～10
3F	***00000	1～5

Maximum Character Number and Icon Display Number in CG RAM

Icon Disp. Number	Max. Chara Number	Note
No Use	8 Chara.	
40 Icons	7 Chara.	$(07)_H$ and $(0F)_H$ can not use for Character Memory.
80 Icons	6 Chara.	$(06)_H$,$(07)_H$,$(0E)_H$ and $(0F)_H$ can not use for Character Memory.

Note2) When the icon display function using, the system should be initialized by the software initialization because of the CG RAM does not initialize except the software initialization.

Maximum Icon Display Number

Line	Digit	Extention Driver	Max. Icon Disp.Number	Line	Digit	Extention Driver	Max. Icon Disp.Number
2	16	No Use	40	4	8	No Use	40
	24	NJU6407C, NJU6407CR	60		16	NJU6407C, NJU6407CR	80
	32	NJU6407C, NJU6407CR	80		20	NJU6417C	80
	40	NJU6417C	80		24	NJU6415, NJU6416	80

(1−8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits operation.
RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.
Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.
This circuit also generates to control signals for the extension driver NJU6407C, 6417C or 6416.

(1−9) LCD Driver

LCD driver consist of 33-common driver and 40-segment driver.
When the line number is selected by a program, the required common drivers output the common driving waveform and the other common drivers output non-selection waveform automatically.
The 40 bits of character pattern data are shifted in the shift-register and latched when the 40 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1−10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.
The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).
When the address counter is $(08)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
(AC)	0	0	0	1	0	0	0

2-line Display (← Display position; ← DD RAM address (Hexadecimal))

1	2	3	4	5	6	7	8	9	10	11	12
00	01	02	03	04	05	06	07	<u>08</u>	09	0A	0B
40	41	42	43	44	45	46	47	48	49	4A	4B

↑ Cursor position

4-line Display (← Display position; ← DD RAM address (Hexadecimal))

1	2	3	4	5	6	7	8	9	10	11	12
00	01	02	03	04	05	06	07	<u>08</u>	09	0A	0B
20	21	22	23	24	25	26	27	28	29	2A	2B
40	41	42	43	44	45	46	47	48	49	4A	4B
60	61	62	63	64	65	66	67	68	69	6A	6B

↑ Cursor position

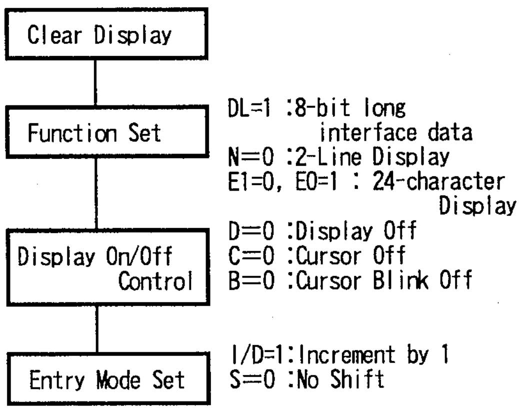
(Note) The cursor or blinks also appear when the address counter (AC) selects the CG RAM.
But the displayed cursor and blink are meaningless.
If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

(2−1) Initialization By Software

The NJU6426 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after V_{DD} rises to 4.5V.

Initialization flow is shown below:



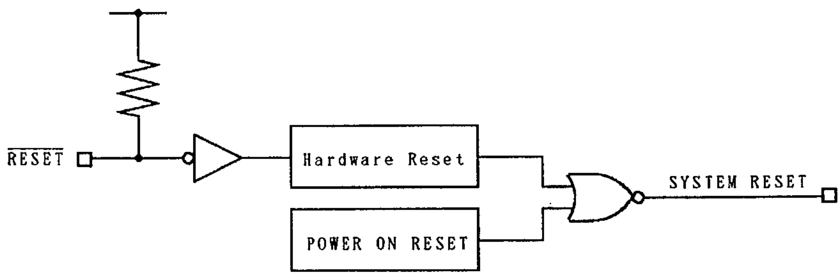
NOTE

If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

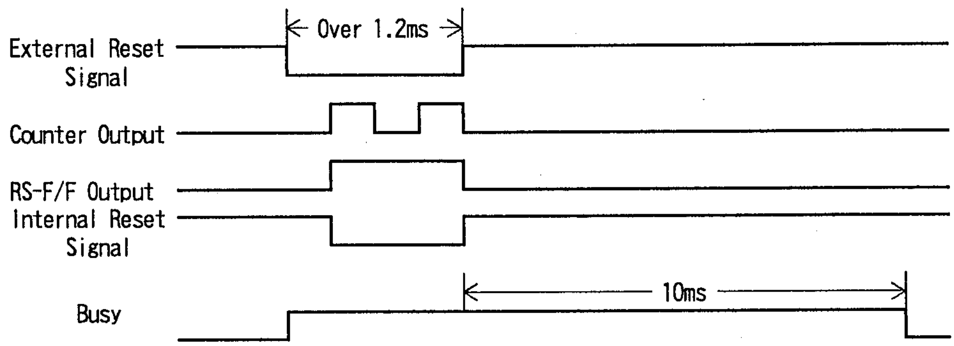
(2−2) Initialization By Hardware

The NJU6426 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 10ms after $\overline{\text{RESET}}$ terminal goes to "H".

・Reset Circuit



・Timing Chart



(3) Instructions

The NJU6426 incorporates two registers, an Instruction Register (IR) and a Data Register (DR). These two registers store control information temporarily to allow interface between NJU6426 and MPU or peripheral ICs operating different cycles. The operation of NJU6426 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).
Table 4. shows each instruction and its operating time.

Note 1) The execution time mentioned in Table 4. based on fcp or fosc=330kHz.
If the oscillation frequency is changed, the execution time is also changed.
Note 2) When the reset function is executed, 40-character 2-line is selected.

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DESCRIPTION	EXEC TIME
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	30us
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	1.48ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged	1.48ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift	30us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	30us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	45us
Function Set	0	0	0	0	1	DL	N	*	E_1	E_0	Sets interface data length(DL), number of display lines(N) and display character number. Character font is fixed 5 X 7. DL=1 : 8 bits , DL=0 : 4 bits N=1 : 4-line , N=0 : 2-line Please refer (g) for E_0 and E_1.	30us
Set CG RAM Address	0	0	0	1	←——		A_{CG}			——→	Sets CG RAM address. After this instruction, the data is transferred to/from CG RAM.	30us
Set DD RAM Address	0	0	1	←——			A_{DD}			——→	Sets DD RAM address. After this instruction, the data is transferred to/from DD RAM.	30us
Read Busy Flag & Address	0	1	BF	←——			A_C			——→	Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0us
Write Data to CG & DD RAM	1	0	←——			Write Data				——→	Writes data into DD or CG RAMs.	30us
Read Data from CG or DD RAM	1	1	←——			Read Data				——→	Reads data from DD or CG RAMs.	45us
Explanation of Abbreviation	DD RAM : Display data RAM , CG RAM : Character generator RAM A_{CG} : CG RAM address , A_{DD} : DD RAM address, Corresponds to cursor address AC : Address counter used for both of DD and CG RAMs											

(3－1) Description of each instructions

(a) Maker Testing

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker). Therefore, please avoid all "0" input or no meaning Enable signal input at data "0". (Especially please pay attention the output condition of Enable signal when the power turns on.)

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0.
When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment.
If the cursor or blink are displayed, they are returned to the left end of the LCD (the left end of the 1st line in the 2-line display mode).
The S of entry mode does not change.
Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

5

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

* = Don't care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD (the left end of the 1st line in the 2-line display mode) if the cursor or blink are on the display.
The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting.

5

(e) Display On/Off Control

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

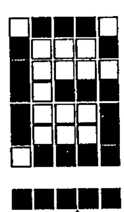
Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 518.4ms at f_{OSC}=330kHz for 24-character 4-line and 433.2ms at f_{CP}=300kHz for others. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.

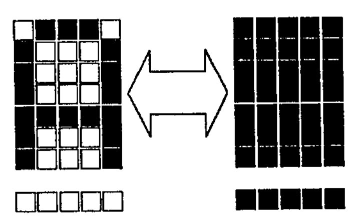
Note) The blink time alters proportionately by $1/f_{OSC}$ or $1/f_{CP}$. For example, when the f_{CP}=300kHz : 518.4 x (330/300) = 570.2ms. (For 24-Character 4-Line)
433.2 x (330/300) = 476.5ms. (For others)



Cursor

Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

5

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In the 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly, each line moves only horizontally.
The 2nd line display does not shift into the 1st line position.
The contents of address counter(AC) does not change by operation of the display shift only.
This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	DL	N	*	E_1	E_0

* = Don't care

Function set instruction which sets the interface data length and number of display lines, is executed when the code "1" is written into DB_5 and the codes of (DL), (N), (E_1) and (E_0) are written into DB_4(DL), DB_3(N), DB_1(E_1) and DB_0(E_0), as shown below (character font is fixed 5 x 7 dots).
(DL) sets the interface data length and (N) sets the number of display lines either the 2-line or 4-line and (E_1), (E_0) select the display character number.

NOTE
This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length to 8 bits (DB_7 to DB_0)
0	Set the interface data length to 4 bits (DB_7 to DB_4) The data must be sent or received twice in this mode.

N	E1	E0	Display lines	Display Digit	Extension Driver
0	0	0	2-line	16 Character	-
	0	1		24 Character	NJU6407C, NJU6407CR
	1	0		32 Character	NJU6407C, NJU6407CR
	1	1		40 Character	NJU6417C
1	*	0	4-line	20 Character	NJU6417C
	*	1		24 Character	NJU6416, NJU6415

(h) Set CG RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	1	A	A	A	A	A	A

←Higher order bit   Lower order bit →

Set CG RAM address set instruction is executed when the code "1" is written into DB_6 and the address is written into DB_5 to DB_0 as shown above.

The address data mentioned by binary code " AAAAAA " is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM.

(i) Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A

←Higher order bit   Lower order bit→

Set DD RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data mentioned by binary code " AAAAAAA " is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the DD RAM.

Note : In case of the 2-line display(N=0), the address data is $(00)_H$ to $(27)_H$ for the 1st line and $(40)_H$ to $(67)_H$ for the 2nd line. And in the 20-character 4-line display(N=1, E0=0), the 「AAAAAAA」 is $(00)_H$ to $(13)_H$ for the 1st line, $(20)_H$ to $(33)_H$ for the 2nd line, $(40)_H$ to $(53)_H$ for the 3rd line and $(60)_H$ to$(73)_H$ for the 4th line. However, in case of the 24-character 4-line(N=1, E0=1), the 「AAAAAAA」 is $(00)_H$ to $(17)_H$ for the 1st line, $(20)_H$ to $(37)_H$ for the 2nd line, $(40)_H$ to $(57)_H$ for the 3rd line and $(60)_H$ to $(77)_H$ for the 4th line.

Display	1st Line	2nd Line	3rd Line	4th Line
2-Line	$(00)_H$ - $(27)_H$	$(40)_H$ - $(67)_H$	-	-
20-Char. 4-Line	$(00)_H$ - $(13)_H$	$(20)_H$ - $(33)_H$	$(40)_H$ - $(53)_H$	$(60)_H$ - $(73)_H$
24-Char. 4-Line	$(00)_H$ - $(17)_H$	$(20)_H$ - $(37)_H$	$(40)_H$ - $(57)_H$	$(60)_H$ - $(77)_H$

(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A

←Higher order bit   Lower order bit→

This instruction reads out the internal status of the NJU6426. When this instruction is executed, the busy flag (BF) which indicate internal operation is read out from DB_7 and the address of the CG RAM or DD RAM is read out from DB_6 to DB_0 (the address for the CG RAM or DD RAM is determined by the previous instruction).

(BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(k) Write Data to CG RAM or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D

←Higher order bit　　　　Lower order bit→

Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 8 bit data " DDDDDDDD " are written into the CG RAM or DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(l) Read Data from CG RAM or DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D

←Higher order bit　　　　Lower order bit→

Read Data from CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 8 bit data " DDDDDDDD " are read out from the CG RAM or DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

Note: The address counter(AC) is automatically incremented or decremented by 1 after write instruction to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(3−2) Initialization using the internal reset circuits

(a) 16-character 2-line display in 8-bit operation (Using internal reset circuits).

At the 16-character 2-line display, the Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

The DD RAM of the NJU6426 can store up to 96 or 80 characters, as explained before, therefore the advertising moving display is available when combined with the display shift operation. Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.

Step	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Remarks
Power On											Initialized. No display appears.
↓ Function Set	0	0	0	0	1	1	0	*	0	0	Set the 8-bit operation, 16-character 2-line display, 5 x 7 dots Font.
↓ Disp.On/Off Cont	0	0	0	0	0	0	1	1	1	0	Turns on display and cursor. Entire display is in space mode set by the initialization.
↓ Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.
↓ Write data to the DD/CG RAM and set the Instruction											

(b) 16-character 2-line in 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full.

16-character 2-line in 4-bit operation is shown as follows:

Step	RS	R/W	DB_7	DB_6	DB_5	DB_4	Description
Power On							Initialized. No display appears.
↓ Function Set	0	0	0	0	1	0	Set the 4-bit operation. This step is executed in 8-bit mode set by the initialization.
↓ Function Set	0	0	0	0	1	0	Set the 4-bit operation 16-character 2-line display, 5 x 7 dots Font. The 4-bit operation starts from this step.
	0	0	0	*	0	0	
↓ Disp.On/Off Cont	0	0	0	0	0	0	Turn on display and cursor. Entire display is in space mode set by the initialization.
	0	0	1	1	1	0	
↓ Entry Mode Set	0	0	0	0	0	0	Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.
	0	0	0	1	1	0	
↓ Write data to the DD/CG RAM and set the Instruction							

(c) 20-character 4-line in 8-bit operation (Using internal reset circuits).
From 1st to 4th line displays will shift at the same time.

Step	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description
Power On											Initialized. No display appears.
↓ Function Set	0	0	0	0	1	1	1	*	*	0	Set the 8-bit operation, 20-character 4-line display, 5 x 7 dots Font.
↓ Disp.On/Off Cont	0	0	0	0	0	0	1	1	1	0	Turns on display and cursor. Entire display is in space mode set by the initialization.
↓ Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data
↓ Write data to the DD/CG RAM and set the Instruction											

5

(3−3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6426 must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface length.

Power On

Initialized.
No display appears.

↓

Wait more than 15ms after V_{DD} rises to 4.5V

↓

Function Set

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

Function Set
(8-bit interface length)

↓

Wait more than 4.1ms

↓

Function Set

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

Function Set
(8-bit interface length)

↓

Wait more than 100us

↓

Function Set

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

Function Set
(8-bit interface length)

Busy Flag(BF) can not be checked before this step, but it can be checked after this step.
After this step, busy flag(BF) check or longer waiting time than each instruction execution time is required.

↓

Function Set

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	1	*	*	1

Set the 8-bit operation, 24-character 4-line display, 5 x 7 dots Font.

↓

Display Off

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	1	0	0	0

↓

Display Clear

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	0	0	1

↓

Entry Mode Set

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	0	0	0	1	1	0

Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.

↓

Write data to the DD/CG RAM and set the Instruction

(b) Initialization by Instruction in 4-bit interface length

Step	RS	R/W	DB_7	DB_6	DB_5	DB_4	Notes
Power On							Initialized. No display appears.
↓ Wait more than 15ms after V_{DD} rises to 4.5V							
↓ Function Set	0	0	0	0	1	1	Function Set (8-bit interface length)
↓ Wait more than 4.1ms							
↓ Function Set	0	0	0	0	1	1	Function Set (8-bit interface length)
↓ Wait more than 100us							
↓ Function Set	0	0	0	0	1	1	Function Set (8-bit interface length) Busy Flag (BF) can not be checked before this step, but it can be checked after this step. After this step, busy flag (BF) check or longer waiting time than each instruction execution time is required.
↓ Function Set	0	0	0	0	1	0	Function Set Set 4-bit interface length by 8-bit interface length.
↓ Function Set	0 0	0 0	0 0	0 *	1 1	0 1	Set the 4-bit operation, 40-character 2-line display 5 x 7 dots Font.
↓ Display Off	0 0	0 0	0 1	0 0	0 0	0 0	
↓ Display Clear	0 0	0 0	0 0	0 0	0 0	0 1	
↓ Entry Mode Set	0 0	0 0	0 0	0 1	0 1	0 0	Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.
↓ Write data to the DD/CG RAM and set the Instruction							

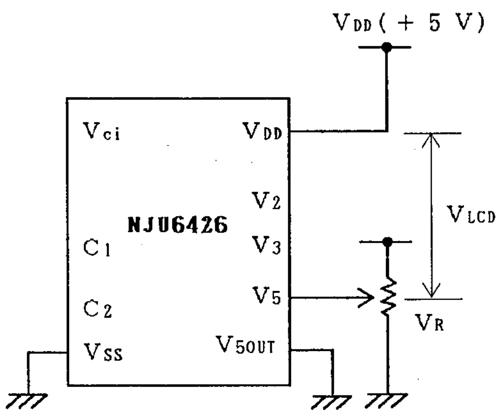
(4) LCD DISPLAY

(4－1) Power Supply for LCD Driving

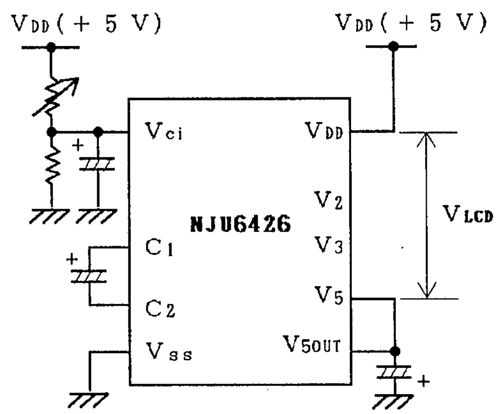
NJU6426 incorporate voltage doubler to generate LCD driving high voltage and bleeder resistance. The voltage doubler generate about twofold voltage from the V_{ci} input voltage (9.5V typ at Iout=2mA and V_{ci}=5V) and bleeder resistance generate each LCD driving voltage. The bleeder resistance is set 1/6 bias suitable for 1/36 duty ratio and each resistance value are 1kΩ typ for R_1, R_2, R_4 and R_5, and 2kΩ typ for R_3.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/36
	Bias	1/6
V_{5OUT}		V_{DD} to V_{LCD}



(a) 1/6 Bias(1/36 Duty)
(Voltage Doubler unused example)

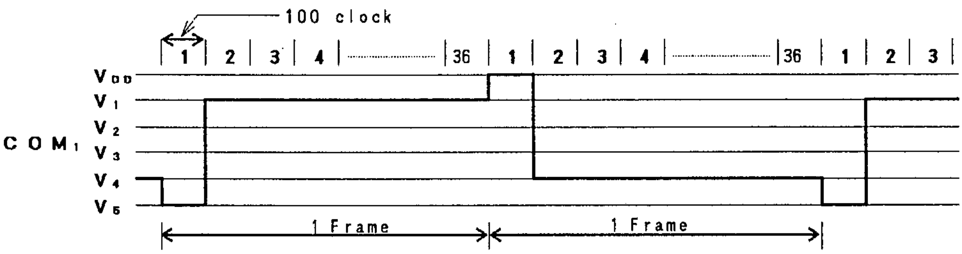


(b) 1/6 Bias(1/36 Duty)
(Voltage Doubler used example)

(4-2) Relation between oscillation frequency and LCD frame frequency.

As the NJU6426 incorporate oscillation capacitor and resistance for CR oscillation, 330kHz oscillation is available without any external components.
The LCD frame frequency example mentioned below is based on 330kHz oscillation.
(1 clock = 3.0us)

1/36 duty



20-character 4-line Display :

1 frame = 3.0(us) x 100 x 36 = 10.8(ms)
Frame frequency = 1/10.8(ms) = 92.6(Hz)

24-character 4-line Display :

1 frame = 3.0(us) x 120 x 36 = 13(ms)
Frame frequency = 1/13.0(ms) = 76.9(Hz)

(5) Interface with MPU

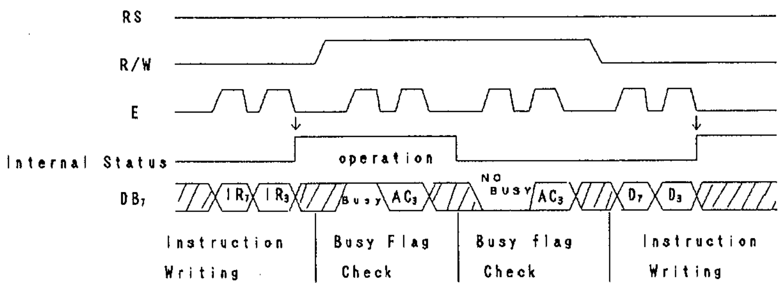
NJU6426 can be interfaced with both of 4/8-bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

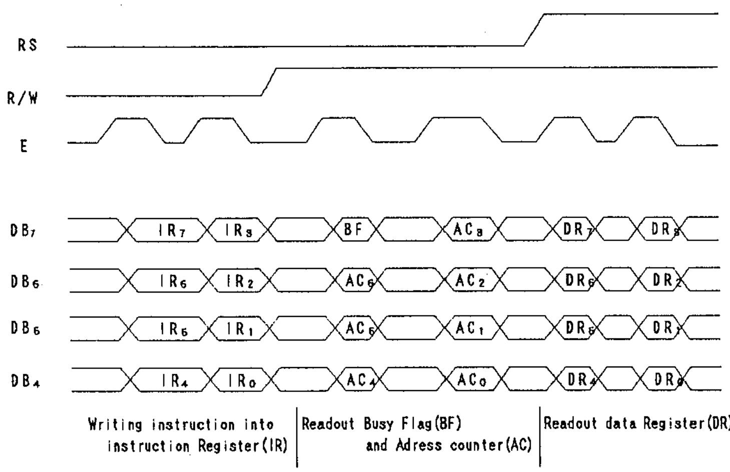
(5−1) 4-bit MPU interface

When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

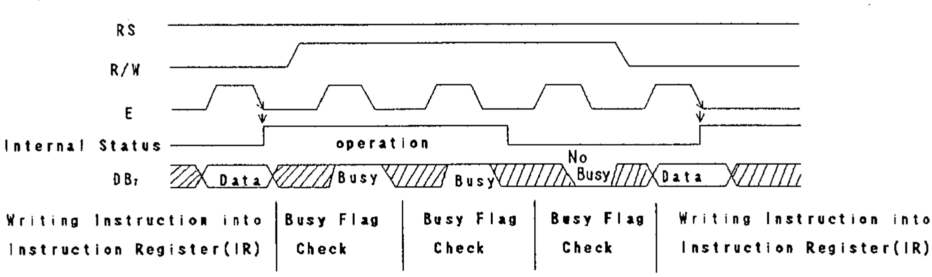
The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check must be executed after two-time 4bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.





(5−2) 8-bit MPU interface



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V
Input Voltage	Vr	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recomended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor riliability.

Note 2) All voltage values are specified as V_{SS} = 0V

Note 3) The relation : $V_{DD} \geqq V_{ci} > V_5 \geqq V_{5OUT}$, V_{SS}=0V must be maintained.
Turn on V_{DD} and V_{ci} at same time or turn on V_{DD} first then turn on V_{ci} must be required.
If the turn on sequence does not meet above conditions, latch up will occur.

Note 4) Decoupling capacitor(C_D) should be connected between V_{ci} and V_{SS} due to the stabilized operation for the voltage doubler.

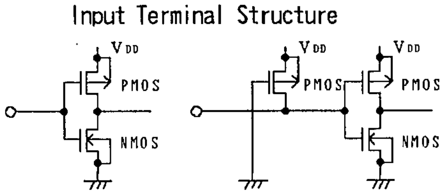
■ ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±10% , Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating Voltage		V_{DD}			4.5	5.0	5.5	V	
Input Voltage		V_{IH}			2.3		V_{DD}	V	5
		V_{IL}					0.8		
Output Voltage		V_{OH}	$-I_{OH}$=0.205mA		2.4			V	6
		V_{OL}	I_{OL}=1.6mA				0.4		
Driver On-resist.(COM)		R_{COM}	±Id=0.05mA(All com.term.)				10	kΩ	9
Driver On-resist.(SEG)		R_{SEG}	±Id=0.05mA(All seg.term.)				10		
Input Leakage Current		I_{LI}	V_{IN}=0 ~ V_{DD}		- 1		1	uA	7
Pull-up Resist Current		$-I_P$	V_{DD}=5V,RS,R/W,DB Terminals		50	125	250		
Operating Current		I_{DD}	V_{DD}=5V, f_{osc}=330kHz			2.0	4.0	mA	8
Voltage Doubler	Output Voltage	V_{up}	Ta=25°C V_{5OUT} Terminal	I_{OUT}=5mA	-3.0	-4.0		V	
				I_{OUT}=1mA	-4.6	-4.8			
	Input Volt.	V_{ci}	—		2.5		5.5	V	
	Conv. Effici	V_{ef}	R_L=∞		95.0	99.9		%	
Built-in Bleeder resistance (For LCD Driving Voltage)		R_1	Ta=25°C			1.00		kΩ	
		R_2				1.00			
		R_3				2.00			
		R_4				1.00			
		R_5				1.00			
Oscillation Frequency		f_{osc}	V_{DD}=5V, Ta=25°C		280	330	390	kHz	
LCD Driving Voltage		V_{LCD}	V_{5OUT} Terminal, V_{DD}=5V		V_{DD}-3.0		V_{DD}-13.5	V	10

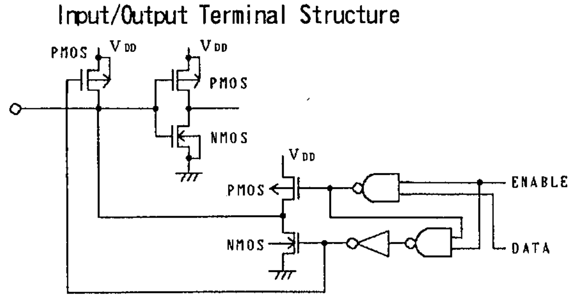
Note 5) Input/Output structure except LCD driver are shown below:

Input Terminal Structure



E Terminal RS,R/W Terminals

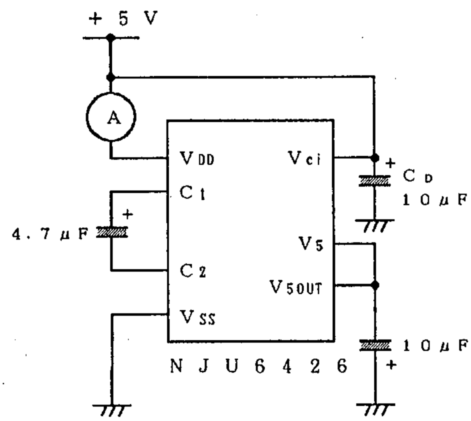
Input/Output Terminal Structure



DB_0 to DB_7 Terminals

Note 6) Apply to the Output and Input/Output Terminal.
Note 7) Except pull-up resistance current and output driver current.
Note 8) Except Input/output current but including the current flow on bleeder resistance.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

Operating Current Measurement Circuit



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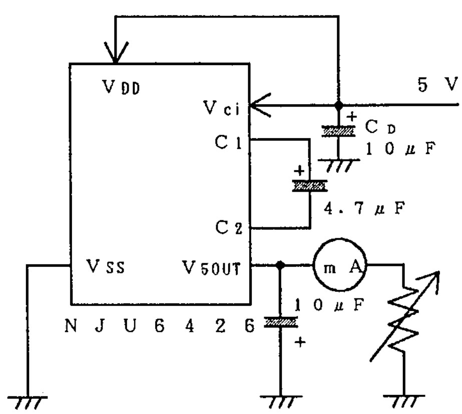
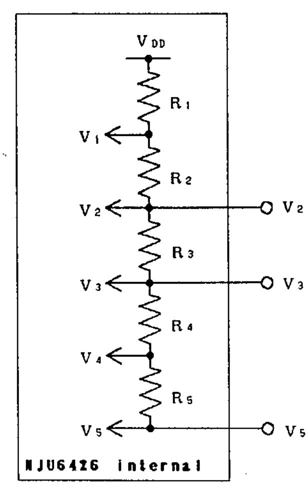
Note 9) R_{COM} and R_{SEG} are the resistance values between power supply terminals (V_{DD}, V_{5OUT}) and each common terminal(COM_1 to COM_{33}), and supply voltage (V_{DD}, V_{5OUT}) and each segment terminal(SEG_1 to SEG_{40}) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.
Note10) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD}, V_1, V_2, V_3, V_4, V_5) at no load condition.

Voltage Doubler Measurement Circuit



Internal Bleeder Resistance



* Voltage Doubler Internal Clock Frequency = 10 ~ 5kHz

- Bus timing characteristics (V_{DD} = 5.0V±10%, V_{SS} = 0V, Ta = -20 ~ +75℃)

Write operation (Write from MPU to NJU6426)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	500		fig.1	ns
Enable Pulse Width	"High" level	P_{WEH}	220			
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Set up Time		t_{DSW}	60			
Data Hold Time		t_{H}	10			

Timing Characteristics (Write operation)

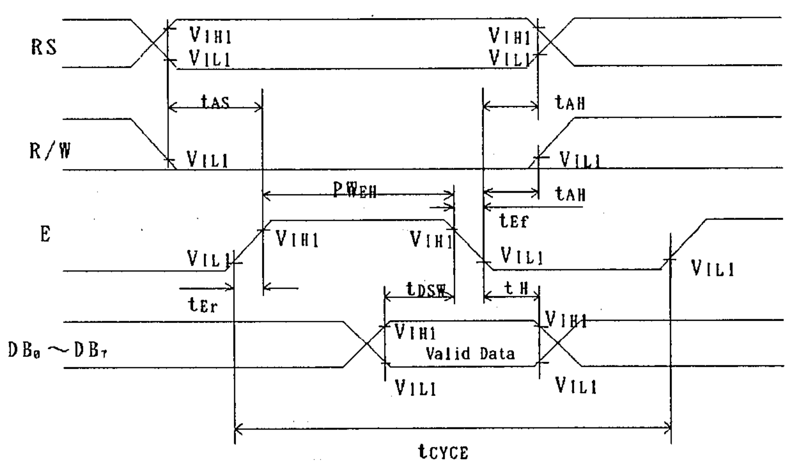


fig. 1

Read operation (Read from NJU6426 to MPU)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable Cycle Time		t_{CYCE}	500		fig.2	ns
Enable Pulse Width	"High" level	P_{WEH}	220			
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}		20		
Set up Time	RS, R/W, E	t_{AS}	40			
Address Hold Time		t_{AH}	10			
Data Delay Time		t_{DDW}		120		
Data Hold Time		t_{DDH}	20			

Timing Characteristics (Read operation)

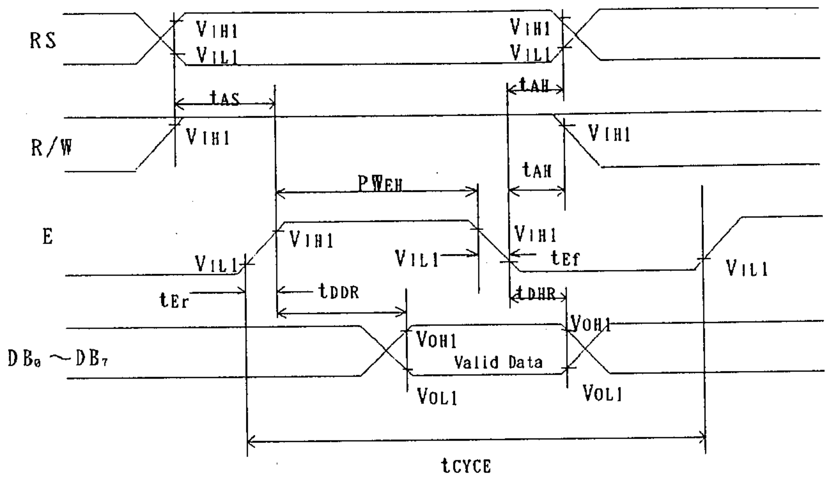


fig. 2

Segment Extension Signal Timing Characteristics (V_{DD}=5.0V±10%,Ta=-20~75℃)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Clock Pulse Width	"High" level	t_{CWH}	800		fig.3	ns
Clock Pulse Width	"Low" level	t_{CWL}	800			
Clock Set up Time		t_{CSU}	500			
Data Set up Time		t_{SU}	300			
Data Hold Time		t_{DH}	300			
M Delay Time		t_{DM}	-1000	1000		
Clock Rise Time, Fall Time		t_{Ct}		100		

Segment Extension Signal Timing

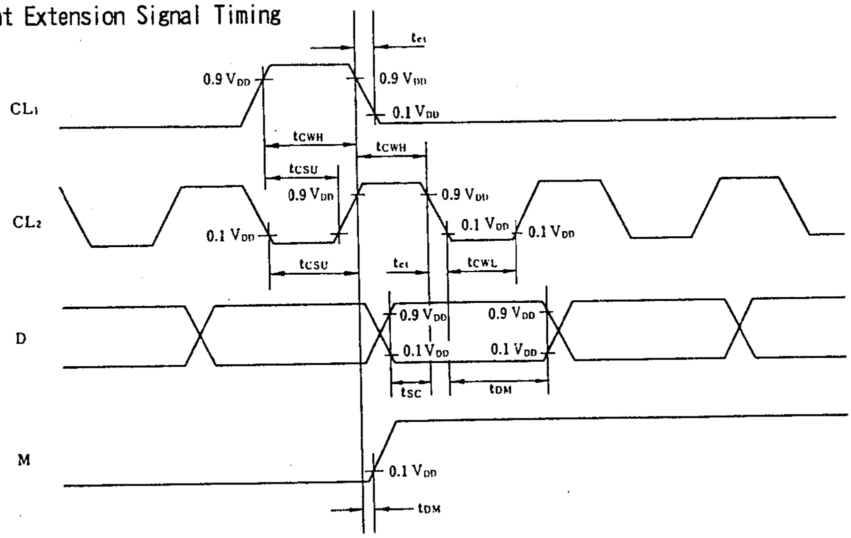
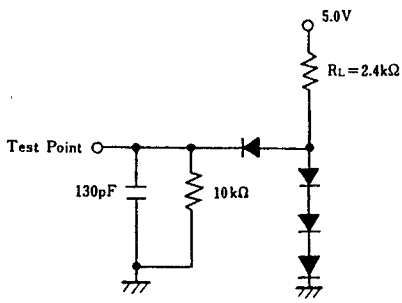
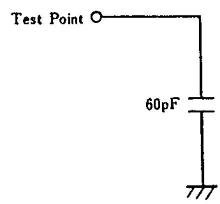


fig. 3

DB0 to DB7 load circuit

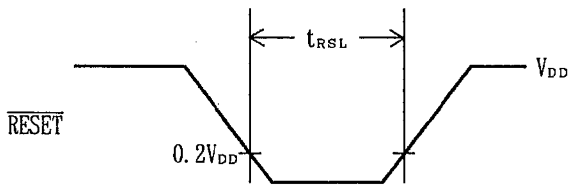


Segment signal load circuit



・The Input Condition when using the Hardware Reset Circuit

Input Timing

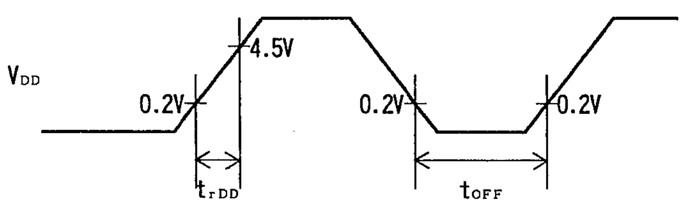


P A R A M E T E R	SYMBOL	MIN	MAX	CONDITION	UNIT
Reset Input "L" Level Width	t_{RSL}	1.2	-	f_{osc}=330kHz	ms

・Power Supply Condition when using the internal initialization circuit(Ta = -20 ～ +75℃)

P A R A M E T E R	SYMBOL	MIN	MAX	CONDITION	UNIT
Power Supply Rise Time	t_{rDD}	0.1	10		ms
Power Supply OFF Time	t_{OFF}	1			

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
(Refer to initialization by the instruction)



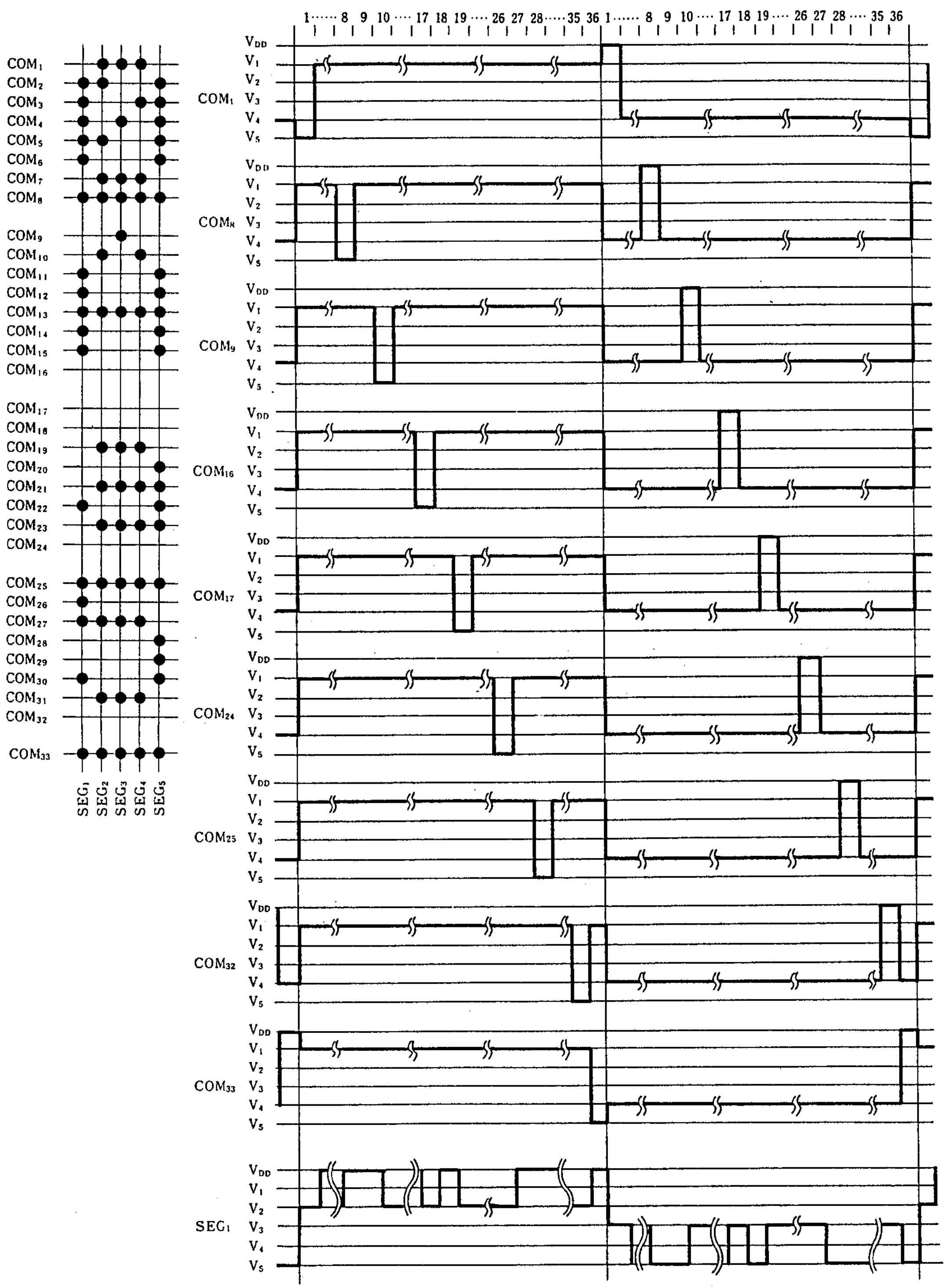
$0.1ms \leqq t_{rDD} \leqq 10ms$ $t_{OFF} \geqq 1ms$

t_{OFF} specifies the power off time in a short period off or cyclical on/off.

5

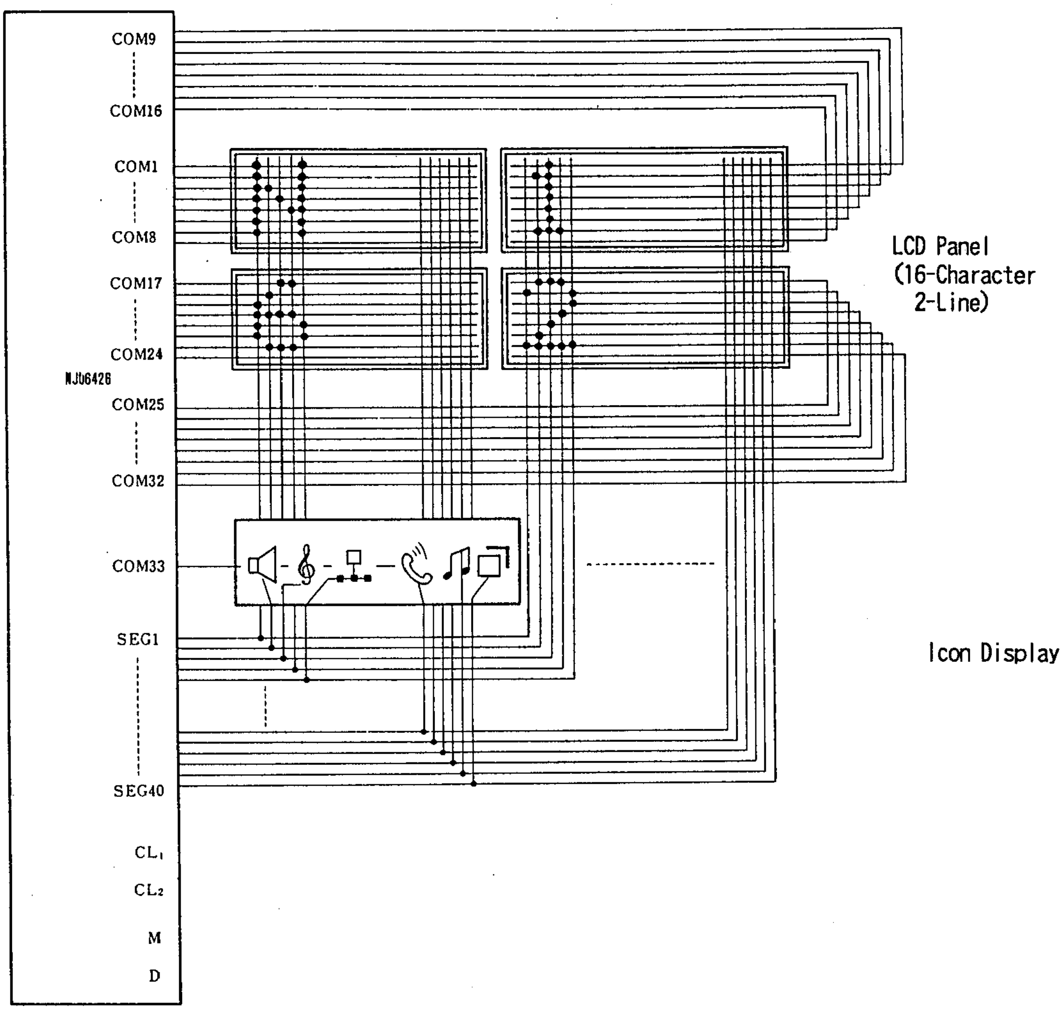
■ LCD DRIVING WAVEFORM

1/36 Duty Driving

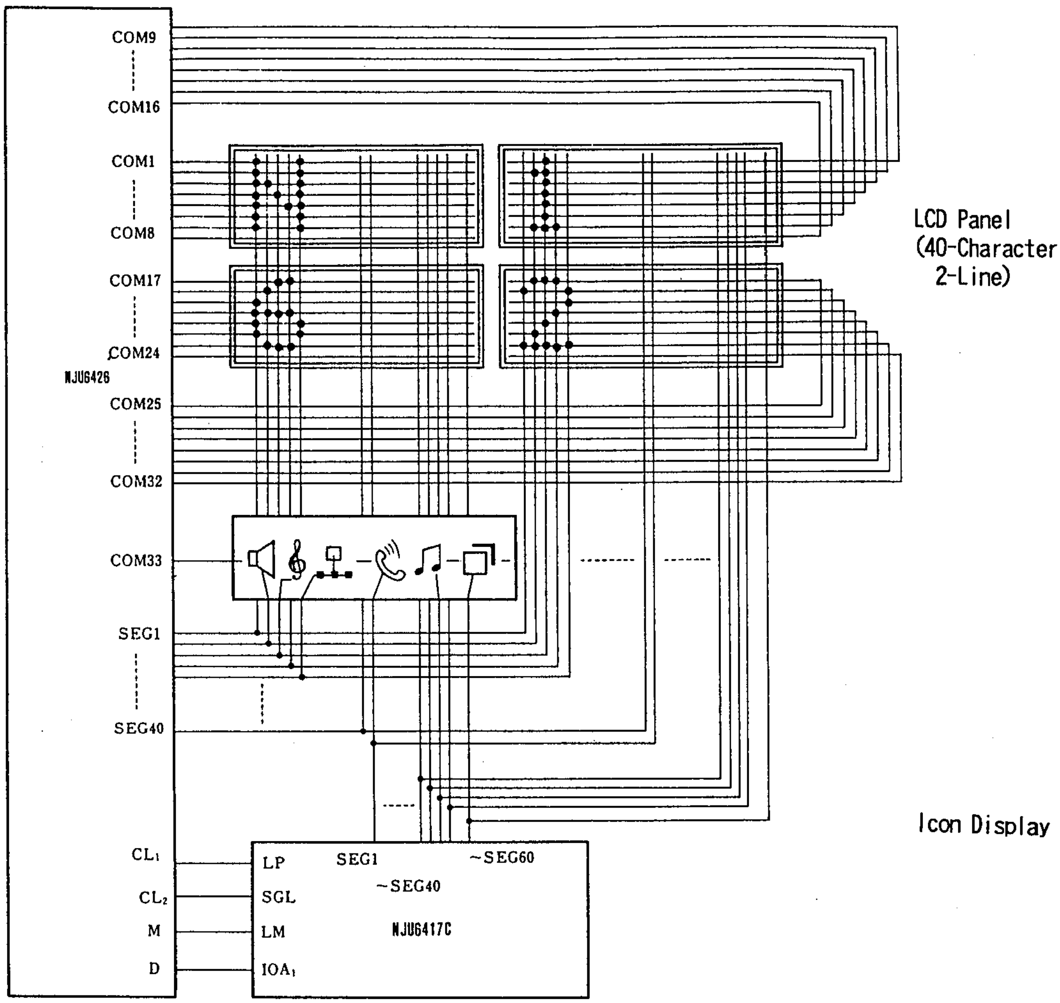


■ APPLICATION CIRCUITS

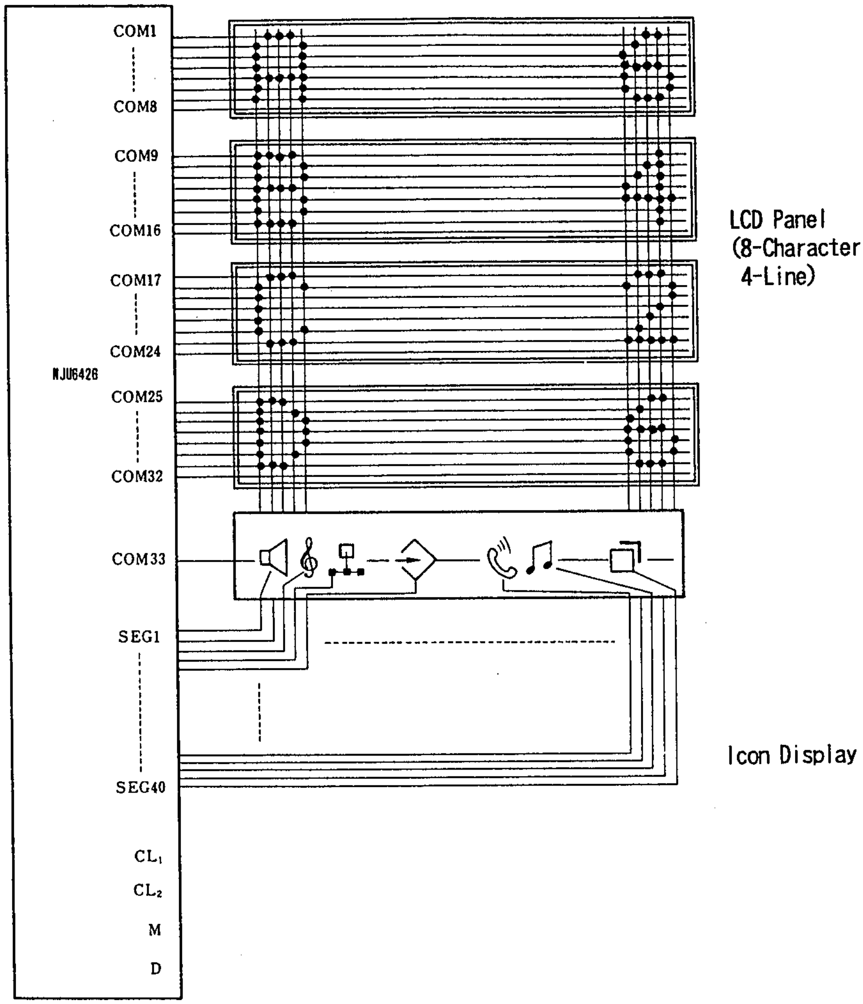
(1) 16-character 2-line Display Example (1/6 Bias, 1/36 Duty)



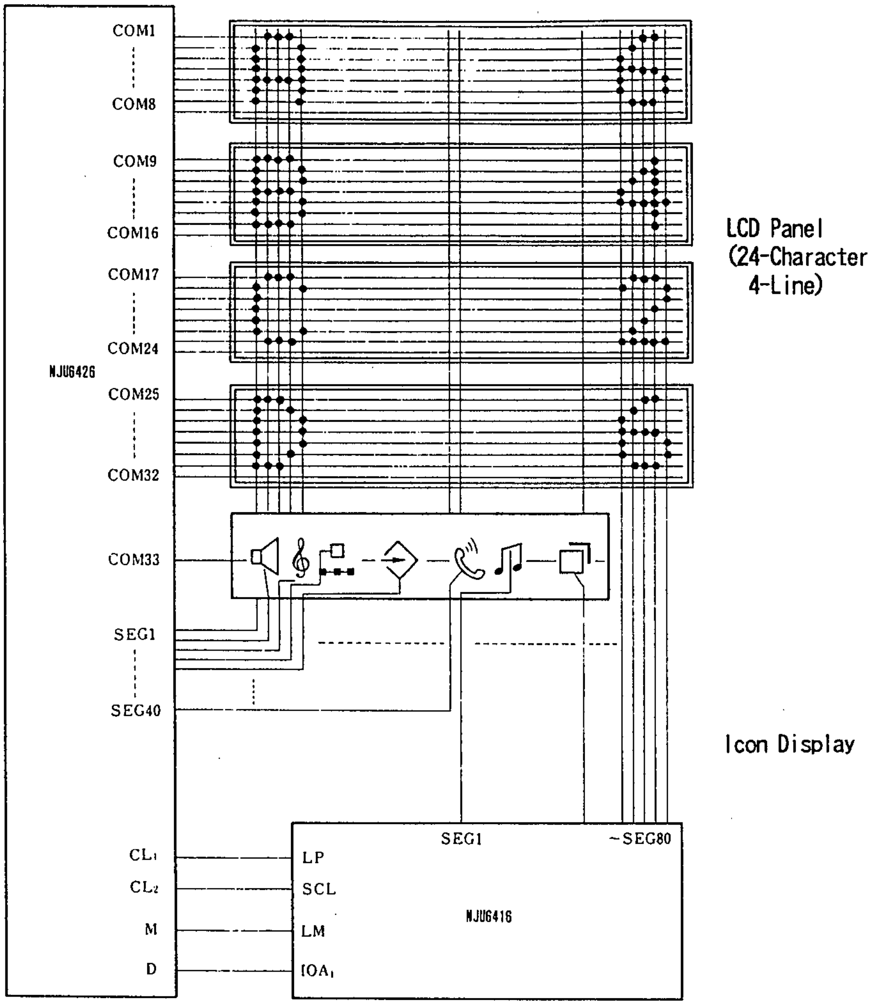
(2) 40-character 2-line Display Example (1/6 Bias, 1/36 Duty)

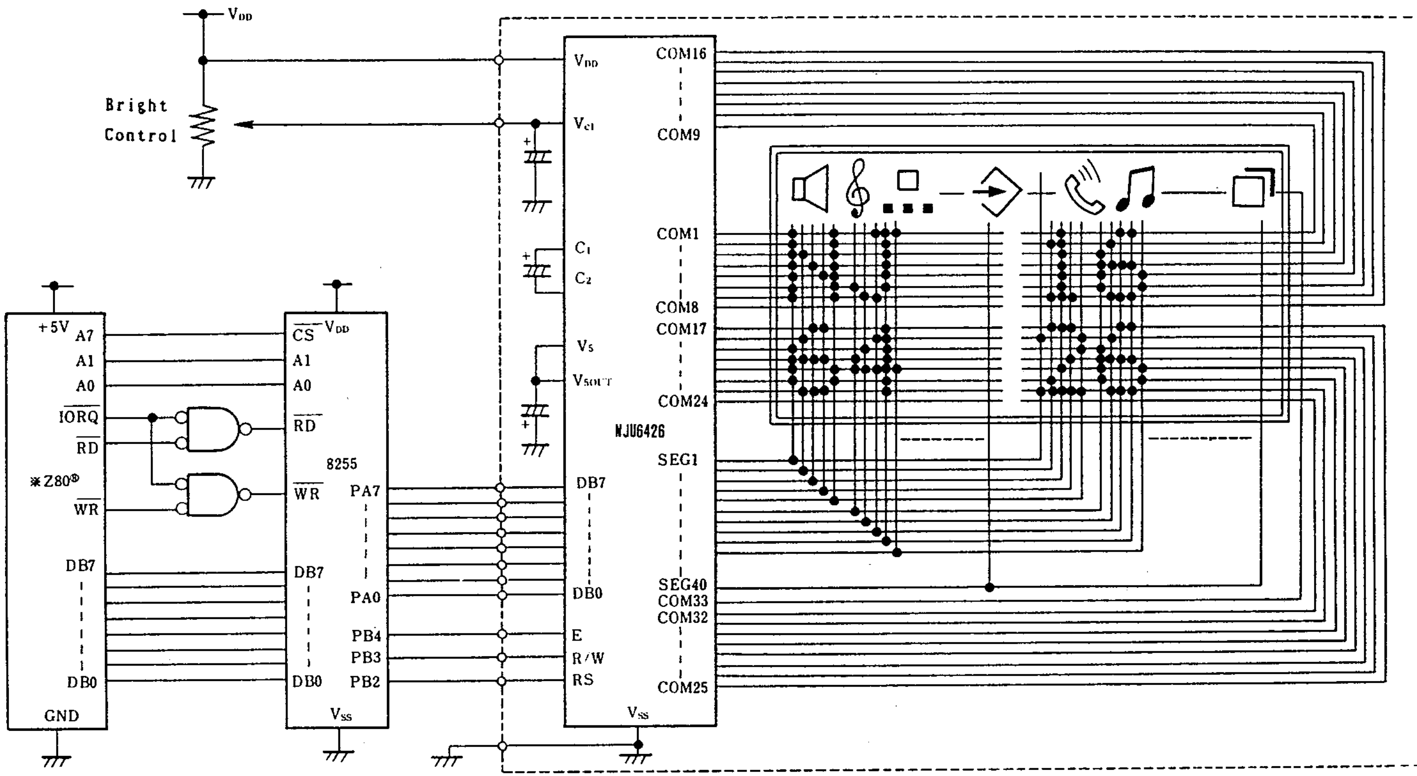


(3) 8-character 4-line Display Example (1/6 Bias, 1/36 Duty)



(4) 24-character 4-line Display Example (1/6 Bias, 1/36 Duty)





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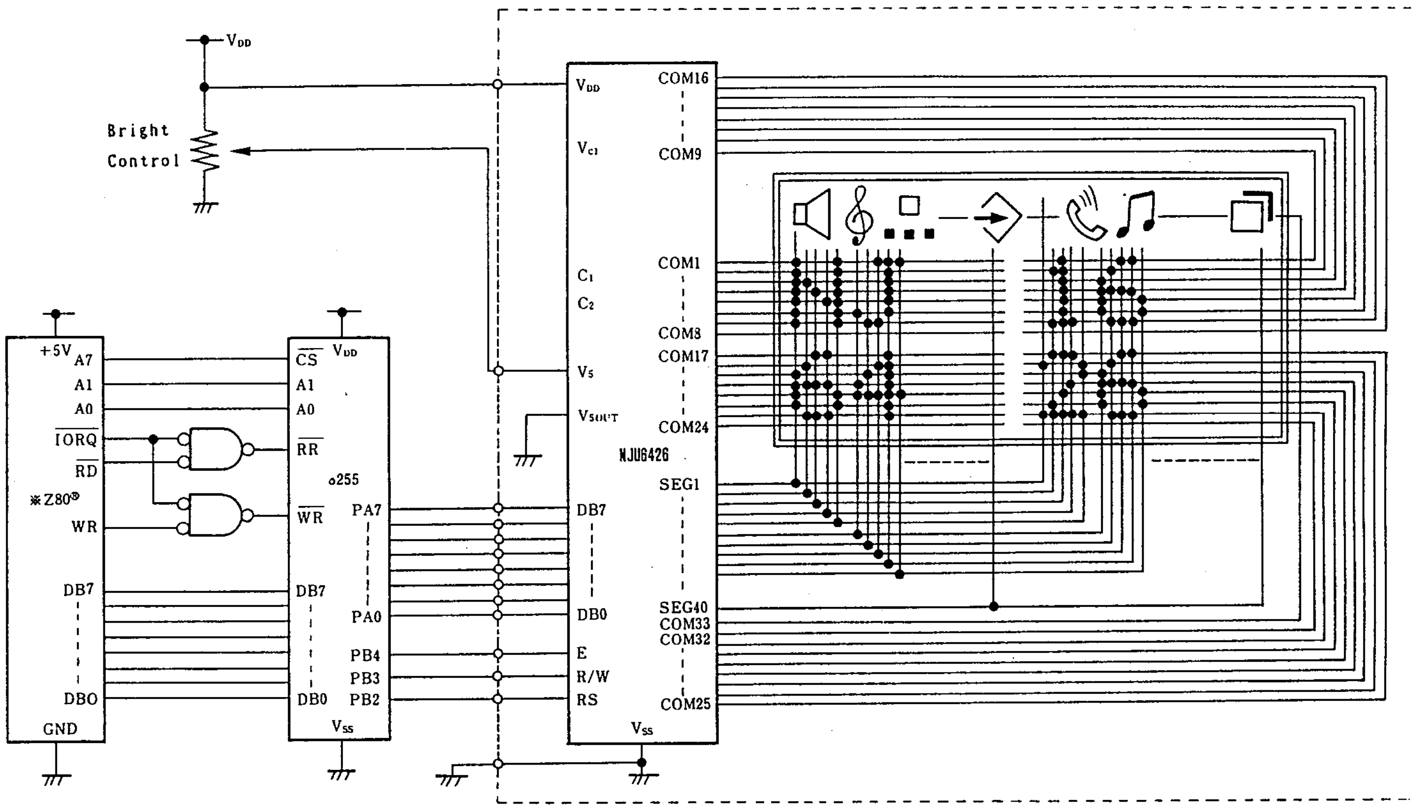
(5) 8 bit MPU interface example (LCD driving voltage is generated by NJU6426)



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(6) 8 bit MPU interface example (LCD driving voltage is supplied from external power supply)

MEMO